WHAT IS CLAIMED IS:

1. A wired-or circuit for a scanable latch, the wired-or circuit comprising:

a first latch coupled to latch a bit during a scan mode;

a second latch;

a first buffer coupled between the first latch and the second latch to propagate the bit via a scan input gate to the second latch during a scan mode and to substantially isolate the scan input gate from the second latch with a first high impedance during a normal input mode; and

a second buffer coupled between the second latch and a normal input gate to propagate data from the normal input gate to the second latch during the normal input mode and to substantially isolate the normal input gate from the second latch with a second high impedance during the scan mode.

2. The apparatus of claim 1, wherein a data signal and a normal input path, evaluation clock are gated directly to the normal input gate to propagate the data from the normal input gate.

3. The apparatus of claim 1, wherein the first buffer comprises a first transistor having a channel coupled between a high voltage output for the scan input gate and the second latch, and a gate controlled by a scan control clock.

4. The apparatus of claim 1, wherein the first buffer comprises a second transistor having a channel coupled between a low voltage output for the scan input gate and the second latch, and a gate controlled by a scan control clock.

5. The apparatus of claim 1, wherein the second buffer comprises a third transistor having a channel coupled between a high voltage source and the second latch, and a gate coupled with an output of the normal input gate.

6. The apparatus of claim 1, wherein the second buffer comprises a fourth transistor having a channel coupled between a low voltage source and the second latch, and a gate coupled with an output of the normal input gate.

7. A wired-or circuit for a scanable latch, the wired-or circuit comprising:
an input latch to latch a bit to a scan path;
an output latch having an input coupled with the scan path and a normal input path;
a first buffer to couple the input latch via a scan input gate to the scan path; and
a second buffer to couple an output of a normal input gate with the normal input path, wherein the first buffer is configured to remain in a high impedance state while data from the output of the normal input gate is propagated to the output latch via the normal input path and the second buffer is configured to remain in the high impedance state while the bit from the input latch is propagated to the output latch via the scan path.

8. The wired-or circuit of claim 7, wherein a data signal and a normal input path, evaluation clock are gated directly to the normal input gate to propagate the data from the output for the normal input gate.

9. The wired-or circuit of claim 7, wherein the first buffer comprises at least two transistors configured to latch a voltage source to the scan path to transmit the bit from the input latch to the output latch.

10. The wired-or circuit of claim 7, wherein the first buffer comprises at least two transistors configured to turn off to substantially isolate the scan path from a voltage source.

11. The wired-or circuit of claim 7, wherein the second buffer comprises at least two transistors configured to latch a voltage source to the normal input path to transmit data from the output of the normal input gate to the output latch.

12. The wired-or circuit of claim 7, wherein the second buffer comprises at least two transistors configured to turn off to substantially isolate the scan path from a voltage source.

13. A normal input gate for gating a data signal to a latch of the scanable latch circuit, the normal input gate comprising:

a pre-charge circuit to pre-charge a dynamic node before the data signal is evaluated;

a logic transistor having a gate coupled with the data signal to discharge the dynamic node when the normal input gate is activated; and

an output to couple a voltage source to the latch based upon a charge on the dynamic node.

14. The normal input gate of claim 13, wherein the data signal and a normal input path, evaluation clock are gated directly to the normal input gate to evaluate the data signal.

15. The normal input gate of claim 13, further comprising a first transistor having a channel coupled between the logic transistor and a low voltage source, and a gate coupled with a comparator to deactivate the normal input gate.

16. The normal input gate of claim 13, further comprising a second transistor having a channel coupled between the output and a low voltage source and a gate coupled with a comparator to deactivate the normal input gate.

17. The normal input gate of claim 13, wherein the output comprises at least two transistors to turn off when in a scan mode, wherein the at least two transistors substantially isolate the normal input gate from the latch when turned off.

18. A scanable latch circuit, comprising:

an output latch;

an input latch having a scan data output;

a normal input gate to output logic data based upon a data signal; and

a wired-or circuit having a first buffer coupled between the output latch and the scan data output to transmit scan data to the output latch during a scan mode and to substantially isolate the output latch from the scan data output with a first high impedance during a normal input mode; and a second buffer coupled between the output latch and an output for the normal input gate to transmit the logic data to the output latch during the normal input mode and to substantially isolate the output latch from the output for the normal input gate with a second high impedance during the scan mode.

19. The scanable latch circuit of claim 18, wherein the normal input gate comprises dynamic logic.

20. The scanable latch circuit of claim 19, further comprising a comparator to determine whether the data signal, upon evaluation by the normal input gate, will change a current state of the output latch.

21. The scanable latch circuit of claim 18, wherein the data signal and a normal input path, evaluation clock are gated directly to the normal input gate to output the logic data.

22. The scanable latch circuit of claim 18, wherein the first buffer comprises a tri-state buffer.

23. A method for switching between scan path and normal input path operations in a scanable latch circuit, the method comprising:

transmitting a data signal to a normal input gate;

transmitting a system clock signal to the normal input gate via a path that is substantially independent of a path to a scan input gate;

evaluating the data signal via the normal input gate; and

turning on a transistor of a normal input, high impedance buffer to couple an output of the normal input gate to an output latch and turning off transistors of a scan input, high impedance buffer, wherein the high impedance buffers are in a normal input mode.

24. The method of claim 23, wherein further comprising turning on a transistor of the scan input, high impedance buffer to couple an input latch via the scan input gate to the output latch and turning off transistors of the normal input, high impedance buffer, wherein the high impedance buffers are in a scan mode.

25. The method of claim 23, further comprising blocking evaluation by the normal input gate based upon the data signal.

26. The method of claim 25, wherein blocking evaluation comprises turning off a blocking transistor coupled between the normal input gate and a low voltage source to prevent a dynamic node of the normal input gate from discharging.

27. The method of claim 26, wherein blocking evaluation comprises comparing the data signal to a current state of the output latch to determine whether the data signal will change the current state.

28. The method of claim 23, wherein transmitting the data signal comprises transmitting the data signal directly to the normal input gate and transmitting the system clock comprises transmitting the system clock directly to the normal input gate.